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| | | Application Number | 09/844,671 |
| | | Filing Date | April 30, 2001 |
| | | First Named Inventor | THEKKATH |
| | | Group Art Unit | 2128 |
| Sheet | 1 of 1 | Examiner Name | Shaawat, Mussa |
| | | Attorney Docket Number | MTEC-002/00US |

| FOREIGN PATENT DOCUMENTS | | | | | | | |
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| Examiner Initials* | Cite No. ¹ | Foreign Patent Document | | | Name of Patentee or Applicant of Cited Document | Date of Publication of Cited Document MM-DD-YYYY | T ⁴ |
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| Examiner Initials* | Cite No. ¹ | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | | | T ² |
| RF | D1 | Susan J. EGGERS, et al., "Techniques for Efficient Inline Tracing on a Shared-Memory Multiprocessor," University of Washington, 1990 ACM, pp. 37-47. | | | |
| RF | D2 | Richard A. UHLIG, et al., "Trace-Driven Memory Simulation: A Survey," Intel Microcomputer Research Lab; University of Michigan, ACM Computing Surveys, Vol. 29, No. 2, June 1997, pp. 128-170. | | | |
| RF | D3 | Eric ROTENBERG, et al., "Trace Processors," University of Wisconsin, 1997 IEEE Service Center, 12 pp. | | | |
| RF | D4 | E.N. ELNOZAHY, "Address Trace Compression Through Loop Detection and Reduction," ©1999 ACM 1-58113-083, pp. 214, 215. | | | |
| RF | D5 | Darren JONES, "Opal Coprocessor Interface," MIP Proprietary/Confidential, June 4, 1999, pp. 1-18. | | | |
| RF | D6 | Darren JONES, MIPSS64™ SKC™ Processor Cores User's Manual, Rev. 1.0, July 4, 1999, pp. 6-1 to 6-26. | | | |
| RF | D7 | MIPSS64™ SKC™ Processor Cores User's Manual, Rev. 1.0.1., 1999, pp. 247-276. | | | |
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| Examiner Signature |  | Date Considered | 13 Sep 05 |
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